ABSTRACT

A ferroelectric memory device having plural memory cells, each composed of a memory cell transistor and a memory cell capacitor including a lower electrode that is independent for each memory cell capacitor, a ferroelectric layer formed on the lower electrode, and an upper electrode layer formed on the ferroelectric layer. A plurality of the upper electrode layers are connected together and constitute a plate electrode, and the width of the upper electrode is narrower than the width of the ferroelectric layer. Accordingly, by making the width of the upper electrode narrower than the width of the ferroelectric layer, it is possible to prevent current leakage between the upper electrode and the lower electrode, which reduces the placement interval of the memory cell capacitors without causing current leakage between the upper electrode and the lower electrode, and results in a smaller memory cell size.